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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,442	03/16/2004	Mutsuo Morikado	790001-2045	2001

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s).	
	10/801,442	MORIKADO, MUTSUO	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *14-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 10-13* is/are rejected.

7)☒ Claim(s) *8 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/16/4; 10/29/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election

1. Applicant's election without traverse of Group I, claims 1-13 in the reply filed on 04/11/05 is acknowledged.

2. Claims 14-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 04/11/05.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 7, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Inaba et al. (U.S. Patent No. 6,525,403 B2).

In re claim 1, Inaba (esp. Fig. 7) discloses a semiconductor device, comprising:

a projecting second semiconductor layer (11A) which is formed on a first semiconductor layer (11);

third and fourth (S/D) semiconductor layers (15, 16) which are formed on the first semiconductor layer to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode (14) which is in contact with the second semiconductor layer with a gate insulating film (13) interposed therebetween and forms a channel in the second semiconductor layer; and

an insulating film (12) which is formed in the first semiconductor layer located immediate under the third and fourth semiconductor layers.

In re claim 2, Inaba discloses the device of claim 1, wherein the insulating film is formed in the first semiconductor layer to surround a region located immediately under the second semiconductor layer.

In re claim 7, Inaba (esp. Fig. 7) discloses a semiconductor device, comprising:

an insulating film (12) formed on a first semiconductor layer;

a projecting second semiconductor layer (11A) which is formed on the insulating film;

third and fourth semiconductor layers (15, 16) which are formed on the insulating film to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode (14) which is in contact with the second semiconductor layer with a gate insulating film (13) interposed therebetween and forms a channel in the second semiconductor layer; and

a connection region (between the two sides of the insulating layer) which is formed immediately under the second semiconductor layer to electrically connect the first semiconductor layer and the second semiconductor layer.

In re claim 10, Inaba discloses the device of claim 7, wherein the third and fourth semiconductor layers (15, 16) are isolated (separated) from the first semiconductor layer by the insulating film.

In re claim 11, Inaba discloses the device of claim 7, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Mathew et al. (US 2003/0151077 A1).

In re claim 1, Mathew (esp. Figs. 8-9) discloses a semiconductor device, comprising:

a projecting second semiconductor layer (18) which is formed on a first semiconductor layer (12);

third and fourth semiconductor layers (18) which are formed on the first semiconductor layer to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode (28) which is in contact with the second semiconductor layer with a gate insulating film (26) interposed therebetween and forms a channel in the second semiconductor layer; and

an insulating film (14) which is formed in the first semiconductor layer located immediate under the third and fourth semiconductor layers.

In re claim 3, Mathew discloses the device of claim 1, wherein the third and fourth semiconductor layers are isolated from the first semiconductor layer by the insulating film.

In re claim 4, Mathew discloses the device of claim 1, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

4. Claims 1-4, 7, 10 and 11 rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent No. 6,885,055 B2).

In re claim 1, Lee (esp. Fig. 3b) discloses a semiconductor device, comprising:

a projecting second semiconductor layer (4) which is formed on a first semiconductor layer (2b);

third and fourth semiconductor layers (column 5, lines 48-51) which are formed on the first semiconductor layer to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode (16) which is in contact with the second semiconductor layer with a gate insulating film (12) interposed therebetween and forms a channel in the second semiconductor layer; and

an insulating film (10) which is formed in the first semiconductor layer located immediate under the third and fourth semiconductor layers.

In re claim 2, Lee discloses the device of claim 1, wherein the insulating film is formed in the first semiconductor layer to surround a region located immediately under the second semiconductor layer.

In re claim 3, Lee discloses the device of claim 1, wherein the third and fourth semiconductor layers are isolated from the first semiconductor layer by the insulating film.

In re claim 4, Lee discloses the device of claim 1, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

In re claim 7, Lee (esp. Fig. 3b) discloses a semiconductor device, comprising:

an insulating film (10) formed on a first semiconductor layer;

a projecting second semiconductor layer (4) which is formed on the insulating film;

third and fourth semiconductor layers (column 5, lines 48-51) which are formed on the insulating film to be in contact with the second semiconductor layer and oppose each other via the second semiconductor layer;

a gate electrode (16) which is in contact with the second semiconductor layer with a gate insulating film (12) interposed therebetween and forms a channel in the second semiconductor layer; and

a connection region (between the two sides of the insulating layer) which is formed immediately under the second semiconductor layer to electrically connect the first semiconductor layer and the second semiconductor layer.

In re claim 10, Lee discloses the device of claim 7, wherein the third and fourth semiconductor layers (column 5, lines 48-51) are isolated (separated) from the first semiconductor layer by the insulating film.

In re claim 11, Lee discloses the device of claim 7, wherein the gate electrode is formed so its ends oppose each other via the second semiconductor layer in a direction perpendicular to a direction in which the third and fourth semiconductor layers oppose each other.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5, 6, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagasaka et al. (U.S. Patent No. 6,300,683 B1) in view of Lee (as above).

In re claim 5, 6, 12 and 13, Lee discloses the devices of claims 1 and 7 respectively, but does not expressly disclose a deep trench capacitor device coupled thereto. Nagasaka discloses a semiconductor memory device with deep trench capacitor coupled to a MOS transistor comprising:

a cell capacitor which is formed on a semiconductor layer and whose storage node (55) electrode is connected to a source/drain region (61) wherein the cell capacitor comprises

a trench which is formed in a first semiconductor layer,

the storage node electrode (55) which fills the trench with a capacitor insulating film (54) interposed therebetween, and

a plate electrode which is formed in a region around the trench in the first semiconductor layer.

It would have been obvious for one skilled in the art at the time of the invention to combine the teachings of Nagasaka and Lee to form a deep trench capacitor with a Fin FET device for the purpose, for example, of enhancing the transistor characteristics such as driving larger drain current and threshold voltage of Fin FET transistors (teaching reference Fischer et al. (US 2004/0229424 A1; sections [0013] – [0015]).

Allowable Subject Matter

7. Claims 8 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815